600MHz to 1100MHz High Linearity Direct Quadrature Modulator

FEATURES

- **Direct Conversion from Baseband to RF**
- **High OIP3: + 22.4dBm at 900MHz**
- **Low Output Noise Floor at 20MHz Offset:**
  No RF: –158dBm/Hz
  P_{OUT} = 4dBm: –152.7dBm/Hz
- **Low Carrier Leakage: –43.7dBm at 900MHz**
- **High Image Rejection: –49dBc at 900MHz**
- **3 Channel CDMA2000 ACPR: –70.4dBc at 900MHz**
- **Integrated LO Buffer and LO Quadrature Phase Generator**
- **50Ω AC-Coupled Single-ended LO and RF Ports**
- **High Impedance Interface to Baseband Inputs with 2.1V Common Mode Voltage**
- 16-Lead QFN 4mm × 4mm Package

APPLICATIONS

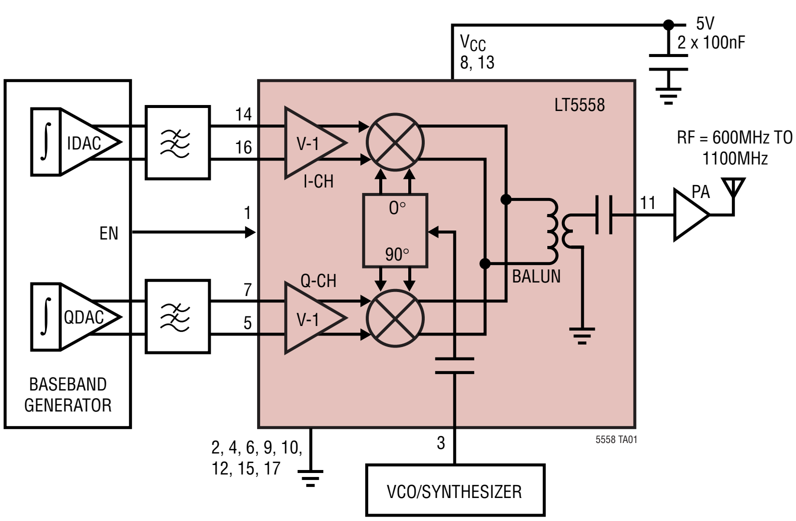
- RFID Single-Sideband Transmitters
- Infrastructure T_X for Cellular and ISM Bands
- Image Reject Up-Converters for Cellular Bands
- Low-Noise Variable Phase-Shifter for 600MHz to 1100MHz Local Oscillator Signals
- Microwave Links

DESCRIPTION

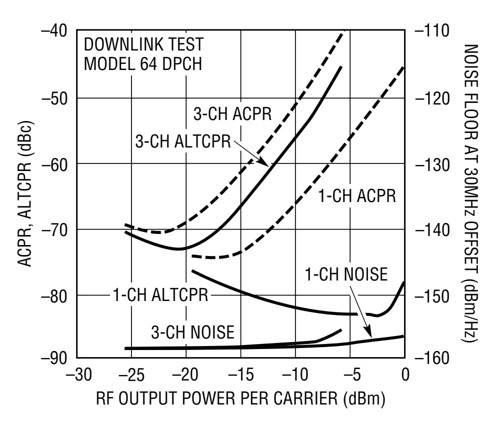
The LT®5558 is a direct I/Q modulator designed for high performance wireless applications, including wireless infrastructure. It allows direct modulation of an RF signal using differential baseband I and Q signals. It supports GSM, EDGE, CDMA, CDMA2000, and other systems. It may also be configured as an image reject upconverting mixer, by applying 90° phase-shifted signals to the I and Q inputs. The high impedance I/Q baseband inputs consist of voltage-to-current converters that in turn drive double-balanced mixers. The outputs of these mixers are summed and applied to an on-chip RF transformer, which converts the differential mixer signals to a 50Ω single-ended output. The balanced I and Q baseband input ports are intended for DC coupling from a source with a common-mode voltage level of about 2.1V. The LO path consists of an LO buffer with single-ended input, and precision quadrature generators which produce the LO drive for the mixers. The supply voltage range is 4.5V to 5.25V.

TYPICAL APPLICATION

600MHz to 1100MHz Direct Conversion Transmitter Application



CDMA2000 ACPR, AltCPR and Noise vs RF Output Power at 900MHz for 1 and 3 Carriers

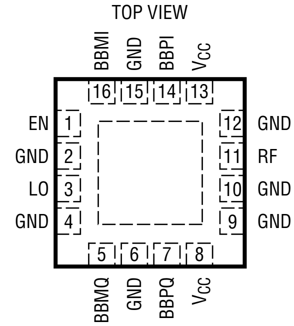


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.5V
Common-Mode Level of BBPI, BBMI and
BBPQ, BBMQ 2.5V
Voltage on any Pin
Not to Exceed....................–500mV to (V_{CC} + 500mV)
Operating Ambient Temperature
(Note 2) ....–40°C to 85°C
Storage Temperature Range...................–65°C to 125°C

PACKAGE/ORDER INFORMATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LT5558EUF

UF PART MARKING
5558

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, f_{RF} = 902MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ CM input voltage = 2.1V_{DC}, baseband input frequency = 2MHz, I and Q 90° shifted (upper sideband selection). $P_{RF(OUT)}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Output (RF)						
f_{RF}	RF Frequency Range	–3 dB Bandwidth –1 dB Bandwidth		600 to 1100 680 to 960		MHz MHz
$S_{22, ON}$	RF Output Return Loss	EN = High (Note 6)		–15.8		dB
$S_{22, OFF}$	RF Output Return Loss	EN = Low (Note 6)		–13.3		dB
NFloor	RF Output Noise Floor	No Input Signal (Note 8) P_{RF} = 4dBm (Note 9) P_{RF} = 4dBm (Note 10)		–158 –152.7 –152.3		dBm/Hz dBm/Hz dBm/Hz
G_P	Conversion Power Gain	$P_{OUT}/P_{IN,I\&Q}$		9.7		dB
G_V	Conversion Voltage Gain	20 • Log ($V_{OUT, 50\Omega}/V_{IN, DIFF, I or Q}$)		–5.1		dB
P_{OUT}	Absolute Output Power	$1V_{P-P DIFF}$ CW Signal, I and Q		–1.1		dBm
$G_{3LO vs LO}$	3 • LO Conversion Gain Difference	(Note 17)		–26.5		dB
OP1dB	Output 1dB Compression	(Note 7)		7.8		dBm
OIP2	Output 2nd Order Intercept	(Notes 13, 14)		65		dBm
OIP3	Output 3rd Order Intercept	(Notes 13, 15)		22.4		dBm
IR	Image Rejection	(Note 16)		–49		dBc
LOFT	Carrier Leakage	EN = High, P_{LO} = 0dBm (Note 16)		–43.7		dBm
	(LO Feedthrough)	EN = Low, P_{LO} = 0dBm (Note 16)		–60		dBm
EVM	GSM Error Vector Magnitude	P_{RF} = 2dBm		0.6		%
LO Input (LO)						
f_{LO}	LO Frequency Range			600 to 1100		MHz
P_{LO}	LO Input Power		–10	0	5	dBm

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, f_{RF} = 902MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ CM input voltage = 2.1V_{DC}, baseband input frequency = 2MHz, I and Q 90° shifted (upper sideband selection). $P_{RF(OUT)}$ = –10dBm, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$S_{11, ON}$	LO Input Return Loss	EN = High (Note 6)		–10.6		dB
$S_{11, OFF}$	LO Input Return Loss	EN = Low (Note 6)		–2.5		dB
NF_{LO}	LO Input Referred Noise Figure	(Note 5) at 900MHz		14.6		dB
G_{LO}	LO to RF Small-Signal Gain	(Note 5) at 900MHz		16.4		dB
$IIP3_{LO}$	LO Input 3rd Order Intercept	(Note 5) at 900MHz		–3.3		dBm
Baseband Inputs (BBPI, BBMI, BBPQ, BBMQ)						
BW_{BB}	Baseband Bandwidth	–3dB Bandwidth		400		MHz
V_{CMBB}	DC Common-mode Voltage	(Note 4)		2.1		V
$R_{IN, DIFF}$	Differential Input Resistance	Between BBPI and BBMI (or BBPQ and BBMQ)		3		kΩ
$R_{IN, CM}$	Common Mode Input Resistance	(Note 20)		100		Ω
$I_{CM, COMP}$	Common Mode Compliance Current range	(Notes 18, 20)		–820 to 440		µA
$P_{LO\text{-}BB}$	Carrier Feedthrough on BB	P_{OUT} = 0 (Note 4)		–46		dBm
IP1dB	Input 1dB compression point	Differential Peak-to-Peak (Notes 7, 19)		3.4		$V_{P\text{-}P,DIFF}$
$\Delta G_{I/Q}$	I/Q Absolute Gain Imbalance			0.05		dB
$\Delta \varphi_{I/Q}$	I/Q Absolute Phase Imbalance			0.2		Deg
Power Supply (V_{CC})						
V_{CC}	Supply Voltage		4.5	5	5.25	V
$I_{CC(ON)}$	Supply Current	EN = High		108	135	mA
$I_{CC(OFF)}$	Supply Current, Sleep mode	EN = 0V		0.1	50	µA
t_{ON}	Turn-On Time	EN = Low to High (Note 11)		0.3		µs
t_{OFF}	Turn-Off Time	EN = High to Low (Note 12)		1.1		µs
Enable (EN), Low = Off, High = On						
Enable	Input High Voltage Input High Current	EN = High EN = 5V	1	 230		V µA
Shutdown	Input Low Voltage	EN = Low			0.5	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Tests are performed as shown in the configuration of Figure 7.

Note 4: At each of the four baseband inputs BBPI, BBMI, BBPQ and BBMQ.

Note 5: V_{BBPI} - V_{BBMI} = 1V_{DC}, V_{BBPQ} - V_{BBMQ} = 1V_{DC}.

Note 6: Maximum value within –1dB bandwidth.

Note 7: An external coupling capacitor is used in the RF output line.

Note 8: At 20MHz offset from the LO signal frequency.

Note 9: At 20MHz offset from the CW signal frequency.

Note 10: At 5MHz offset from the CW signal frequency.

Note 11: RF power is within 10% of final value.

Note 12: RF power is at least 30dB lower than in the ON state.

Note 13: Baseband is driven by 2MHz and 2.1MHz tones. Drive level is set in such a way that the two resulting RF tones are –10dBm each.

Note 14: IM2 measured at LO frequency + 4.1MHz

Note 15: IM3 measured at LO frequency + 1.9MHz and LO frequency + 2.2MHz.

Note 16: Amplitude average of the characterization data set without image or LO feedthrough nulling (unadjusted).

Note 17: The difference in conversion gain between the spurious signal at f = 3 • LO - BB versus the conversion gain at the desired signal at f = LO + BB for BB = 2MHz and LO = 900MHz.

Note 18: Common mode current range where the common mode (CM) feedback loop biases the part properly. The common mode current is the sum of the current flowing into the BBPI (or BBPQ) pin and the current flowing into the BBMI (or BBMQ) pin.

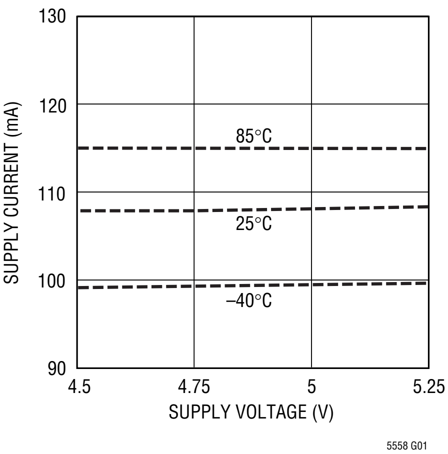
Note 19: The input voltage corresponding to the output P1dB.

Note 20: BBPI and BBMI shorted together (or BBPQ and BBMQ shorted together).

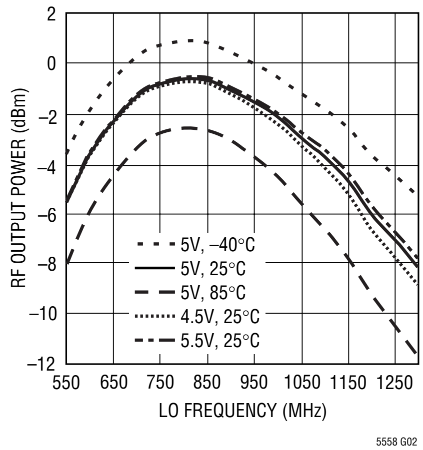
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, f_{RF} = 902MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ CM input voltage = 2.1V_{DC}, baseband input frequency = 2MHz, I and Q 90° shifted, without image or LO feedthrough nulling. f_{RF} = f_{BB} + f_{LO} (upper side-band selection). $P_{RF(OUT)}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

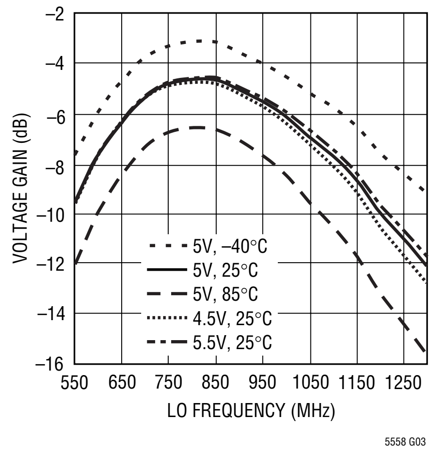
Supply Current vs Supply Voltage



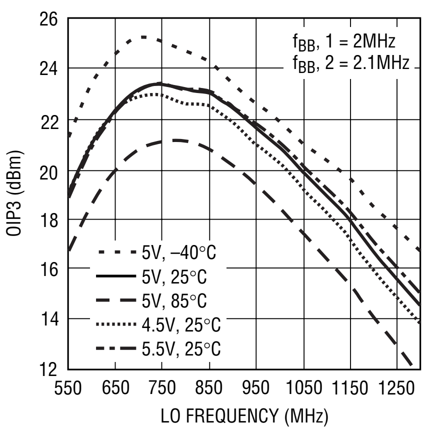
RF Output Power vs LO Frequency at 1V$_{P-P}$ Differential Baseband Drive



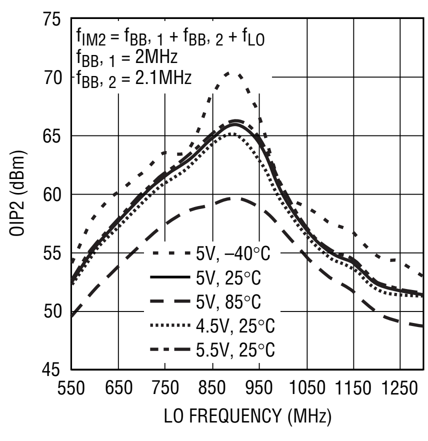
Voltage Gain vs LO Frequency



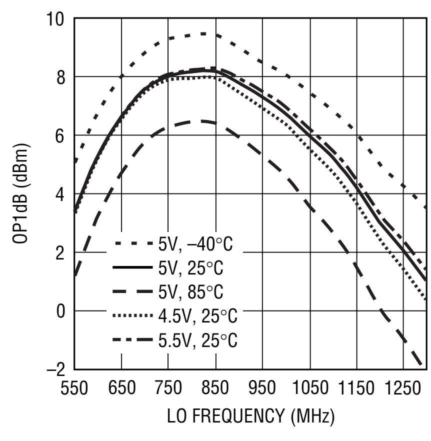
Output IP3 vs LO Frequency



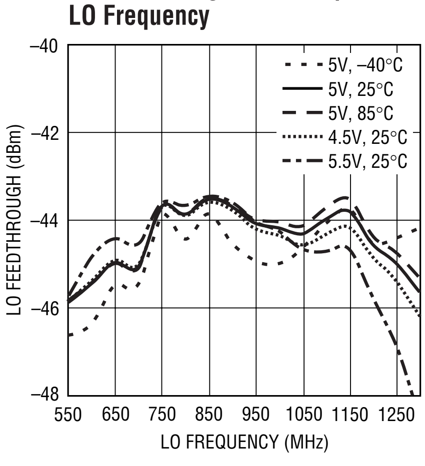
Output IP2 vs LO Frequency



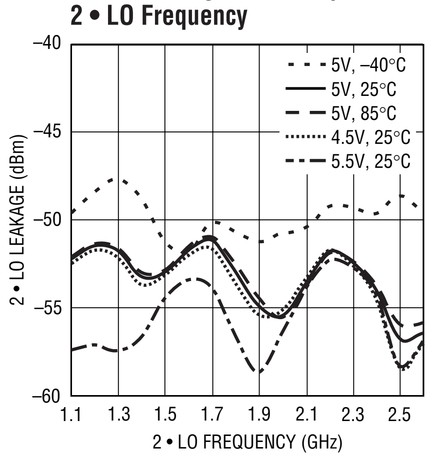
Output 1dB Compression vs LO Frequency



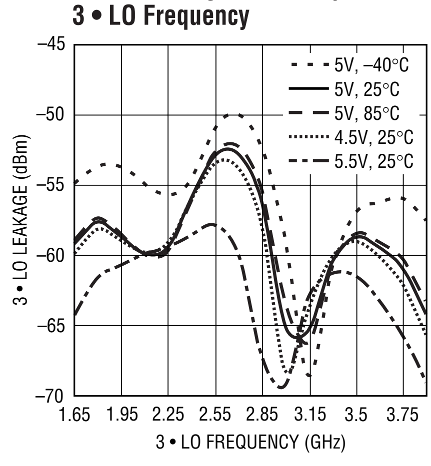
LO Feedthrough to RF Output vs LO Frequency



2 • LO Leakage to RF Output vs 2 • LO Frequency



3 • LO Leakage to RF Output vs 3 • LO Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, EN = High, T_A = 25°C, f_{LO} = 900MHz, f_{RF} = 902MHz, P_{LO} = 0dBm. BBPI, BBMI, BBPQ, BBMQ CM input voltage = 2.1V_{DC}, baseband input frequency = 2MHz, I and Q 90° shifted, without image or LO feedthrough nulling. f_{RF} = f_{BB} + f_{LO} (upper side-band selection). $P_{RF(OUT)}$ = –10dBm (–10dBm/tone for 2-tone measurements), unless otherwise noted. (Note 3)

Noise Floor vs RF Frequency

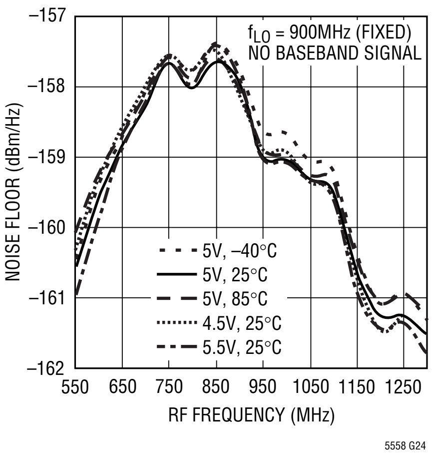
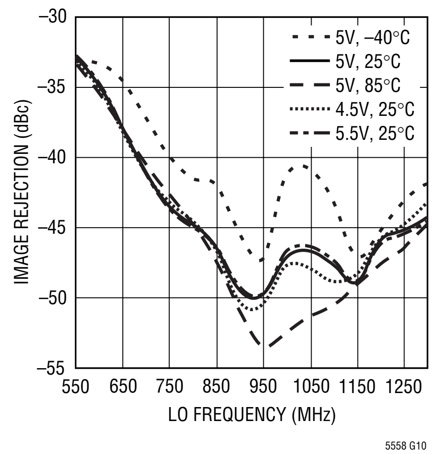
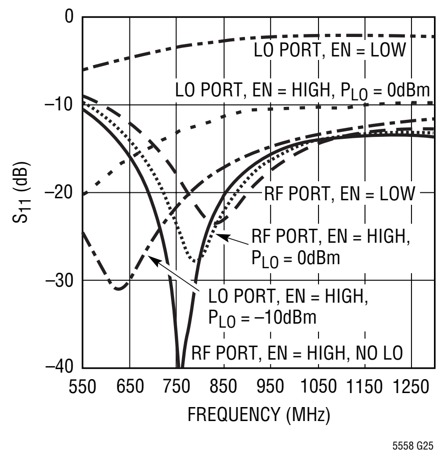


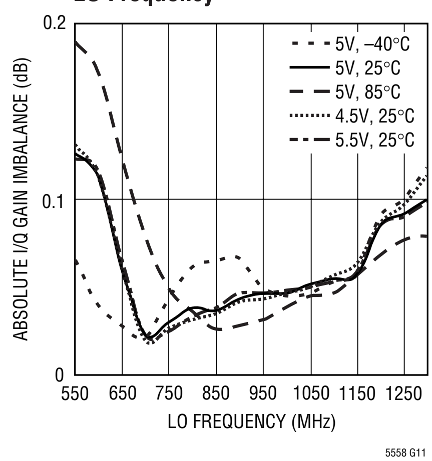
Image Rejection vs LO Frequency



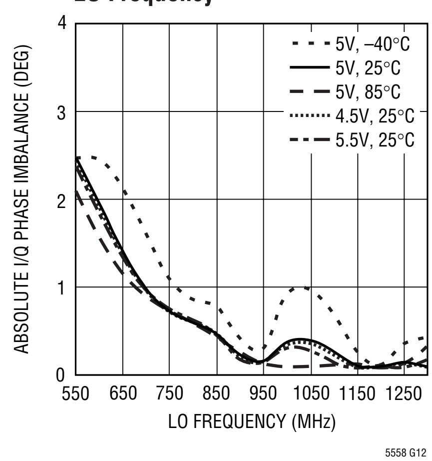
LO and RF Port Return Loss vs RF Frequency



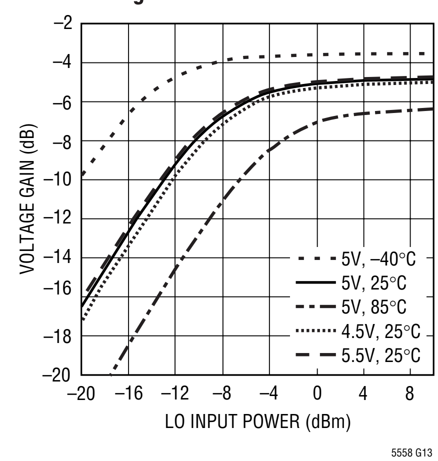
Absolute I/Q Gain Imbalance vs LO Frequency



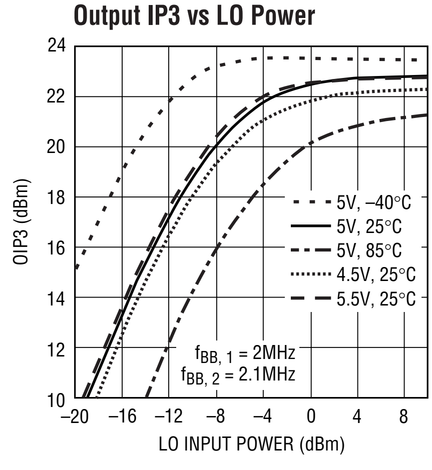
Absolute I/Q Phase Imbalance vs LO Frequency



Voltage Gain vs LO Power



Output IP3 vs LO Power



LO Feedthrough vs LO Power

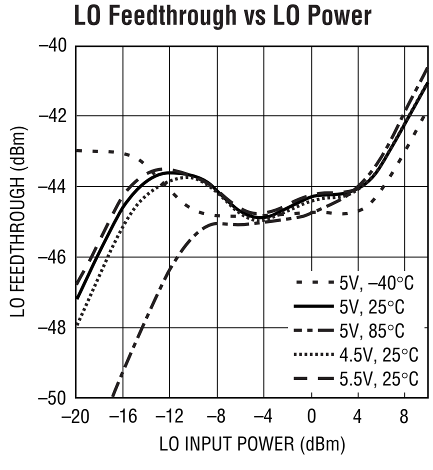
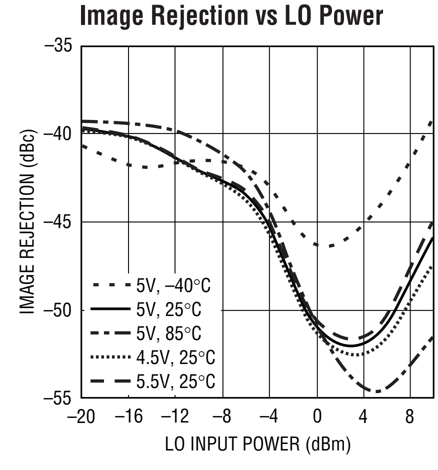


Image Rejection vs LO Power



TYPICAL PERFORMANCE CHARACTERISTICS

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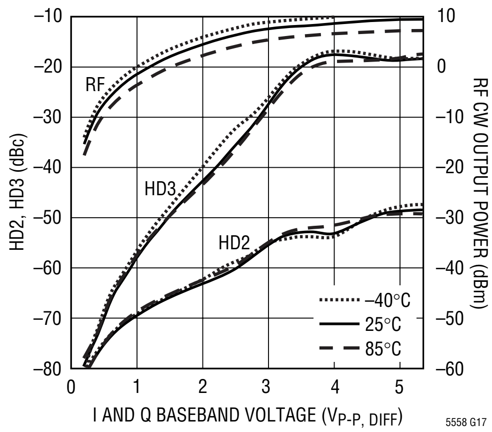
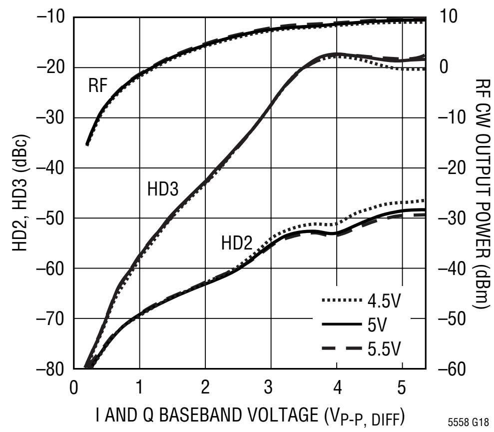
RF CW Output Power, HD2 and HD3 vs CW Baseband Voltage and Temperature



HD2 = MAX POWER AT $f_{LO} + 2 \cdot f_{BB}$ OR $f_{LO} - 2 \cdot f_{BB}$
HD3 = MAX POWER AT $f_{LO} + 3 \cdot f_{BB}$ OR $f_{LO} - 3 \cdot f_{BB}$

RF CW Output Power, HD2 and HD3 vs CW Baseband Voltage and Supply Voltage



HD2 = MAX POWER AT $f_{LO} + 2 \cdot f_{BB}$ OR $f_{LO} - 2 \cdot f_{BB}$
HD3 = MAX POWER AT $f_{LO} + 3 \cdot f_{BB}$ OR $f_{LO} - 3 \cdot f_{BB}$

LO Feedthrough to RF Output vs CW Baseband Voltage

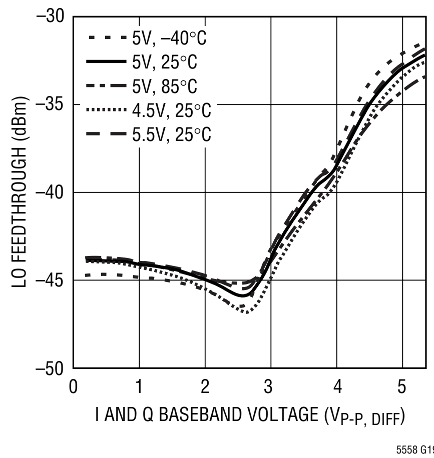
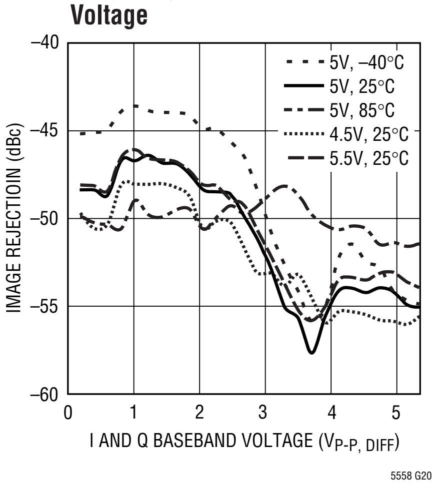
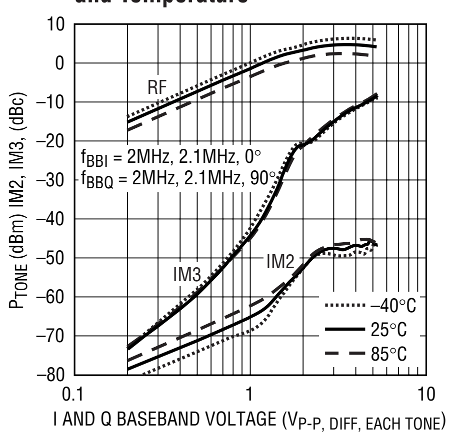


Image Rejection vs CW Baseband Voltage

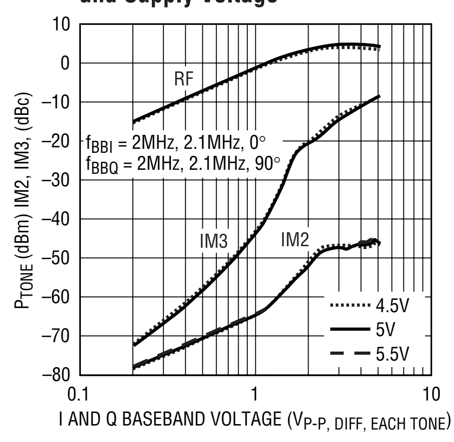


RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Temperature



IM2 = POWER AT f_{LO} + 4.1MHz
IM3 = MAX POWER AT f_{LO} + 1.9MHz OR f_{LO} + 2.2MHz

RF Two-Tone Power (Each Tone), IM2 and IM3 vs Baseband Voltage and Supply Voltage



IM2 = POWER AT f_{LO} + 4.1MHz
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TYPICAL PERFORMANCE CHARACTERISTICS

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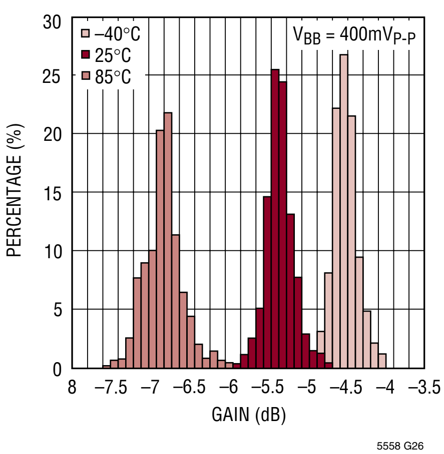
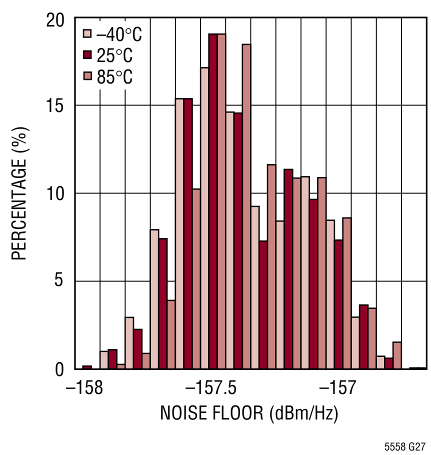
Gain Distribution



Noise Floor Distribution



LO Leakage Distribution

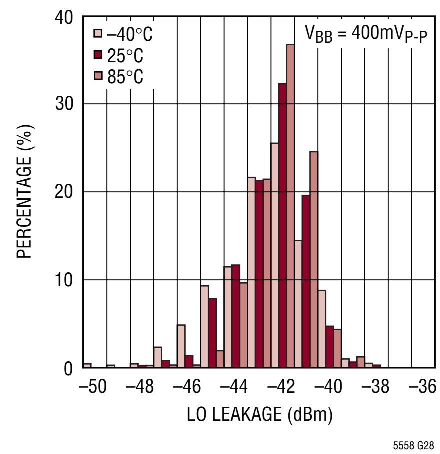
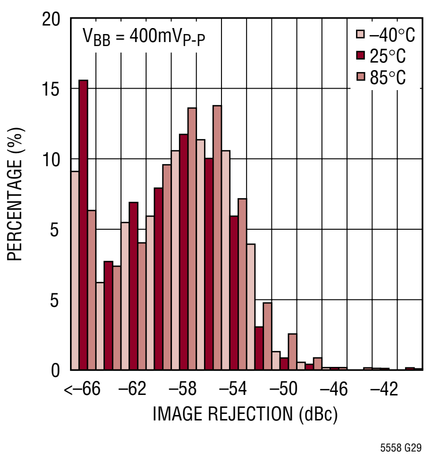
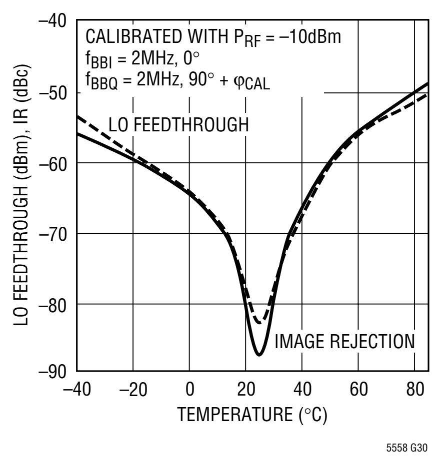


Image Rejection Distribution



LO Feedthrough and Image Rejection vs Temperature After Calibration at 25°C



PIN FUNCTIONS

EN (Pin 1): Enable Input. When the Enable pin voltage is higher than 1V, the IC is turned on. When the Enable voltage is less than 0.5V or if the pin is disconnected, the IC is turned off. The voltage on the Enable pin should never exceed V_{CC} by more than 0.5V, in order to avoid possible damage to the chip.

GND (Pins 2, 4, 6, 9, 10, 12, 15, 17): Ground. Pins 6, 9, 15 and the Exposed Pad, Pin 17, are connected to each other internally. Pins 2 and 4 are connected to each other internally and function as the ground return for the LO signal. Pins 10 and 12 are connected to each other internally and function as the ground return for the on-chip RF balun. For best RF performance, Pins 2, 4, 6, 9, 10, 12, 15 and the Exposed Pad, Pin 17, should be connected to the printed circuit board ground plane.

PIN FUNCTIONS

LO (Pin 3): LO Input. The LO input is an AC-coupled single-ended input with approximately 50Ω input impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to (V_{CC} + 0.5V) in order to avoid turning on ESD protection diodes.

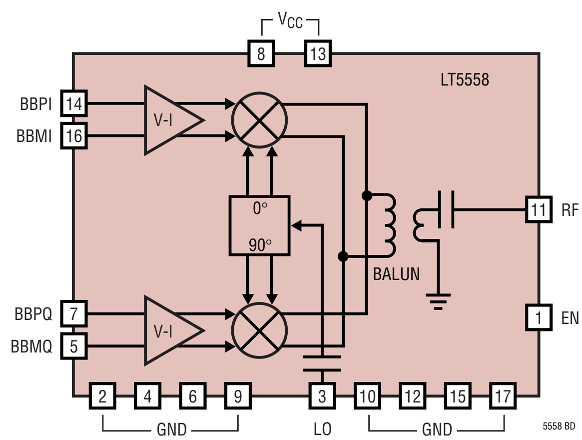
BBPQ, BBMQ (Pins 7, 5): Baseband Inputs for the Q-channel. The differential input impedance is 3kΩ. These pins are internally biased at about 2.1V. Applied common mode voltage must stay below 2.5V.

V_{CC} (Pins 8, 13): Power Supply. Pins 8 and 13 are connected to each other internally. It is recommended to use 0.1μF capacitors for decoupling to ground on each of these pins.

RF (Pin 11): RF Output. The RF output is an AC-coupled single-ended output with approximately 50Ω output impedance at RF frequencies. Externally applied DC voltage should be within the range –0.5V to (V_{CC} + 0.5V) in order to avoid turning on ESD protection diodes.

BBPI, BBMI (Pins 14, 16): Baseband Inputs for the I-channel. The differential input impedance is 3kΩ. These pins are internally biased at about 2.1V. Applied common mode voltage must stay below 2.5V.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT5558 consists of I and Q input differential voltage-to-current converters, I and Q up-conversion mixers, an RF output signal combiner/balun, an LO quadrature phase generator and LO buffers.

External I and Q baseband signals are applied to the differential baseband input pins, BBPI, BBMI, and BBPQ, BBMQ. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced up-converting mixers. The mixer outputs are combined in an RF output balun, which also transforms the output impedance to 50Ω. The center frequency of the resulting RF signal is equal to the LO signal frequency. The LO input drives a phase shifter which splits the LO signal into in-phase and quadrature LO signals. These LO signals are then applied to on-chip buffers which drive the up-conversion mixers. Both the LO input and RF output are single-ended, 50Ω-matched and AC coupled.

Baseband Interface

The baseband inputs (BBPI, BBMI), (BBPQ, BBMQ) present a differential input impedance of about 3kΩ. At each of the four baseband inputs, a low-pass filter using 200Ω and 1.8pF to ground is incorporated (see Figure 1), which limits the baseband –1dB bandwidth to approximately 250MHz. The common-mode voltage is about 2.1V and is slightly temperature dependent. At T_A = -40°C, the common-mode voltage is about 2.28V and at T_A = 85°C it is about 2.01V.

APPLICATIONS INFORMATION

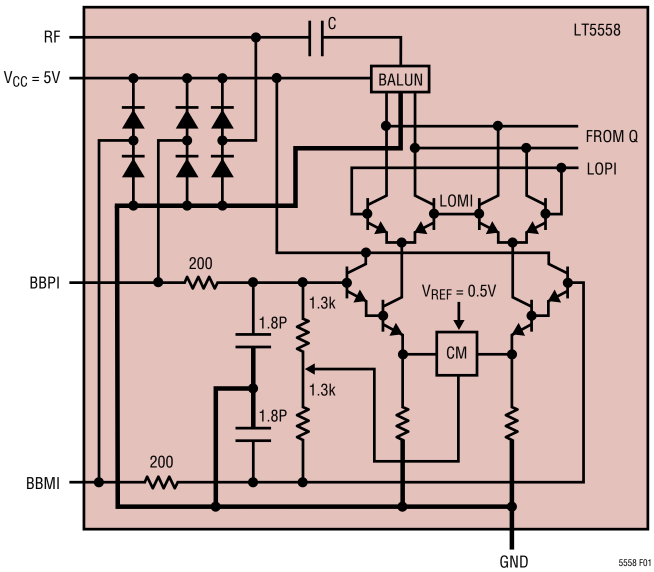


Figure 1. Simplifed Circuit Schematic of the LT5558 (Only I-Half is Drawn)

If the I/Q signals are DC-coupled to the LT5558, it is important that the applied common-mode voltage level of the I and Q inputs is about 2.1V in order to properly bias the LT5558. Some I/Q generators allow setting the common-mode voltage independently. In this case, the common-mode voltage of those generators must be set to 1.05V to match the LT5558 internal bias where the internal DC voltage of the signal generators is set to 2.1V due to the source-load voltage division (See Figure 2).

The LT5558 baseband inputs should be driven differentially, otherwise, the even-order distortion products will degrade the overall linearity severely. Typically, a DAC will be the signal source for the LT5558. A pulse-shaping filter should be placed between the DAC outputs and the LT5558's baseband inputs.

An AC-coupled baseband interface with the LT5558 is drawn in Figure 3. Capacitors C1 to C4 will introduce a

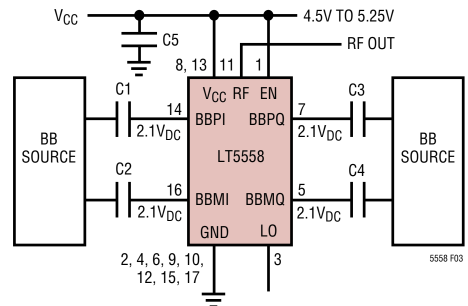


Figure 3. AC-Coupled Baseband Interface

low-frequency high-pass corner together with the LT5558's differential input impedance of 3kΩ. Usually, capacitors C1 to C4 will be chosen equal and in such a way that the –3dB corner frequency $f_{-3dB} = 1/(\pi \cdot R_{IN,DIFF} \cdot C1)$ is much lower than the lowest baseband frequency.

DC coupling between the DAC outputs and the LT5558 baseband inputs is recommended, because AC coupling will introduce a low-frequency time constant that may affect the signal integrity. Active level shifters may be required to adapt the common mode level of the DAC outputs to the common mode input voltage of the LT5558. Such circuits may, however, suffer degraded LO leakage performance as small DC offsets and variations over temperature accumulate. A better scheme is shown in Figure 16, where feedback is used to track out these variations.

LO Section

The internal LO input amplifier performs single-ended to differential conversion of the LO input signal. Figure 4 shows the equivalent circuit schematic of the LO input.

The internal, differential LO signal is split into in-phase and quadrature (90° phase shifted) signals that drive LO buffer sections. These buffers drive the double balanced I and Q mixers. The phase relationship between

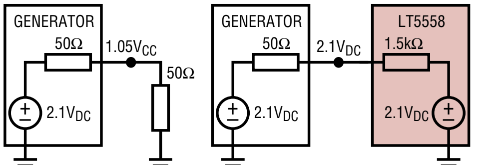


Figure 2. DC Voltage Levels for a Generator Programmed at 1.05VDC for a 50Ω Load and the LT5558 as a Load

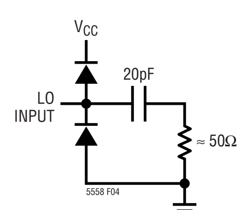


Figure 4. Equivalent Circuit Schematic of the LO Input

APPLICATIONS INFORMATION

the LO input and the internal in-phase LO and quadrature LO signals is fixed, and is independent of start-up conditions. The phase shifters are designed to deliver accurate quadrature signals for an LO frequency near 900MHz. For frequencies significantly below 750MHz or above 1.1GHz, the quadrature accuracy will diminish, causing the image rejection to degrade. The LO pin input impedance is about 50Ω and the recommended LO input power window is –2dBm to + 2dBm. For P_{LO} < –2dBm, the gain, OIP2, OIP3, dynamic-range (in dBc/Hz) and image rejection will degrade, especially at T_A = 85°C.

Harmonics present on the LO signal can degrade the image rejection, because they introduce a small excess phase shift in the internal phase splitter. For the second (at 1.8GHz) and third harmonics (at 2.7GHz) at –20dBc level, the introduced signal at the image frequency is about –61dBc or lower, corresponding to an excess phase shift much less than 1 degree. For the second and third harmonics at –10dBc, still the introduced signal at the image frequency is about –51dBc. Higher harmonics than the third will have less impact. The LO return loss typically will be better than 10dB over the 750MHz to 1GHz range. Table 1 shows the LO port input impedance vs. frequency. The return loss S_{11} on the LO port can be improved at lower frequencies by adding a shunt capacitor.

Table 1. LO Port Input Impedance vs Frequency for EN = High and P_{LO} = 0dBm

FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)	S_{11} MAG	S_{11} ANGLE
500	50.5 + j10.3	0.101	81.3
600	63.8 + j4.6	0.127	16.0
700	70.7 – j6.9	0.180	–15.2
800	70.7 – j20.3	0.237	–34.9
900	63.9 – j30.6	0.285	–50.5
1000	56.7 – j32.2	0.295	–61.4
1100	52.1 – j31.3	0.295	–69.1
1200	46.3 – j32.0	0.318	–78.0

The input impedance of the LO port is different if the part is in shutdown mode. The LO input impedance for EN = Low is given in Table 2.

Table 2. LO Port Input Impedance vs Frequency for EN = Low and P_{LO} = 0dBm

FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)	S_{11} MAG	S_{11} ANGLE
500	37.3 + j43.4	0.464	79.7
600	72.1 + j74.8	0.545	42.1
700	184.7 + j77.8	0.630	11.7
800	203.6 – j120.8	0.696	–12.7
900	75.9 – j131.5	0.737	–32.6
1000	36.7 – j99.0	0.760	–48.8
1100	23.4 – j77.4	0.768	–62.4
1200	17.8 – j62.8	0.764	–74.3

RF Section

After up-conversion, the RF outputs of the I and Q mixers are combined. An on-chip balun performs internal differential to single-ended output conversion, while transforming the output signal impedance to 50Ω. Table 3 shows the RF port output impedance vs frequency.

Table 3. RF Port Output Impedance vs Frequency for EN = High and P_{LO} = 0dBm

FREQUENCY (MHz)	OUTPUT IMPEDANCE (Ω)	S_{22} MAG	S_{22} ANGLE
500	22.8 + j4.9	0.380	165.8
600	30.2 + j11.4	0.283	141.9
700	42.7 + j12.9	0.159	111.8
800	53.7 + j3.0	0.045	37.2
900	52.0 – j10.1	0.101	–73.2
1000	44.8 – j15.2	0.168	–99.7
1100	39.1 – j15.1	0.206	–116.1
1200	35.7 – j13.1	0.224	–128.9

APPLICATIONS INFORMATION

The RF output S22 with no LO power applied is given in Table 4.

Table 4. RF Port Output Impedance vs Frequency for EN = High and No LO Power Applied

FREQUENCY (MHz)(	OUTPUT IMPEDANCE (Ω)	S_{22} MAG	S_{22} ANGLE
500	23.4 + j5.0	0.367	165.5
600	31.7 + j10.7	0.257	142.0
700	44.1 + j9.5	0.118	116.1
800	50.9 – j1.7	0.019	–60.8
900	46.8 – j11.1	0.118	–99.3
1000	40.8 – j13.5	0.178	–115.5
1100	36.6 – j12.6	0.209	–128.1
1200	34.3 – j10.5	0.222	–139.0

For EN = Low the S_{22} is given in Table 5.

To improve S_{22} for lower frequencies, a series capacitor can be added to the RF output. At higher frequencies, a shunt inductor can improve the S_{22}. Figure 5 shows the equivalent circuit schematic of the RF output.

Table 5. RF Port Output Impedance vs Frequency for EN = Low

FREQUENCY (MHz)	OUTPUT IMPEDANCE (Ω)	S_{22} MAG	S_{22} ANGLE
500	21.8 + j4.8	0.398	166.5
600	28.4 + j11.8	0.311	142.9
700	40.2 + j15.4	0.200	112.9
800	54.3 + j8.3	0.090	58.1
900	56.7 – j7.2	0.092	–43.3
1000	49.2 – j15.8	0.158	–83.8
1100	41.9 – j17.0	0.203	–105.0
1200	37.3 – j15.3	0.225	–120.0

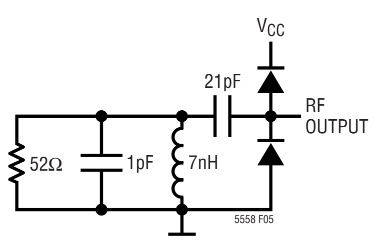


Figure 5. Equivalent Circuit Schematic of the RF Output

Note that an ESD diode is connected internally from the RF output to the ground. For strong output RF signal levels (higher than 3dBm), this ESD diode can degrade the linearity performance if an external 50Ω termination impedance is connected directly to ground. To prevent this, a coupling capacitor can be inserted in the RF output line. This is strongly recommended during 1dB compression measurements.

Enable Interface

Figure 6 shows a simplified schematic of the EN pin interface. The voltage necessary to turn on the LT5558 is 1V. To disable (shut down) the chip, the enable voltage must be below 0.5V. If the EN pin is not connected, the chip is disabled. This EN = Low condition is guaranteed by the 75kΩ on-chip pull-down resistor.

It is important that the voltage at the EN pin does not exceed V_{CC} by more than 0.5V. If this should occur, the full-chip supply current could be sourced through the EN pin ESD protection diodes, which are not designed for this purpose. Damage to the chip may result.

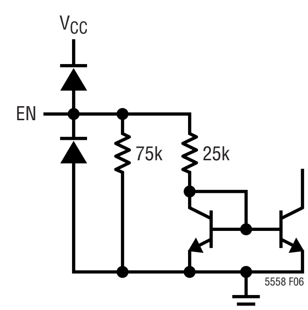


Figure 6. EN Pin Interface

Evaluation Board

Figure 7 shows the evaluation board schematic. A good ground connection is required for the LT5558's Exposed Pad. If this is not done properly, the RF performance will degrade. Additionally, the Exposed Pad provides heat sinking for the part and minimizes the possibility of the chip overheating. R1 (optional) limits the EN pin current in the event that the EN pin is pulled high while the V_{CC} inputs are low. The application board PCB layouts are shown in Figures 8 and 9.

APPLICATIONS INFORMATION

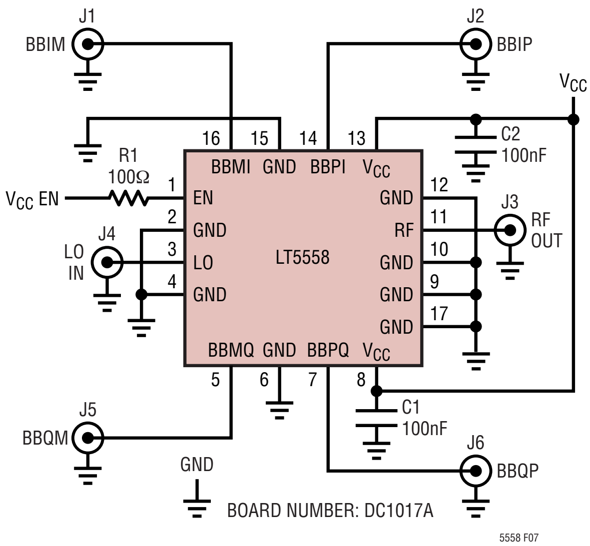


Figure 7. Evaluation Circuit Schematic

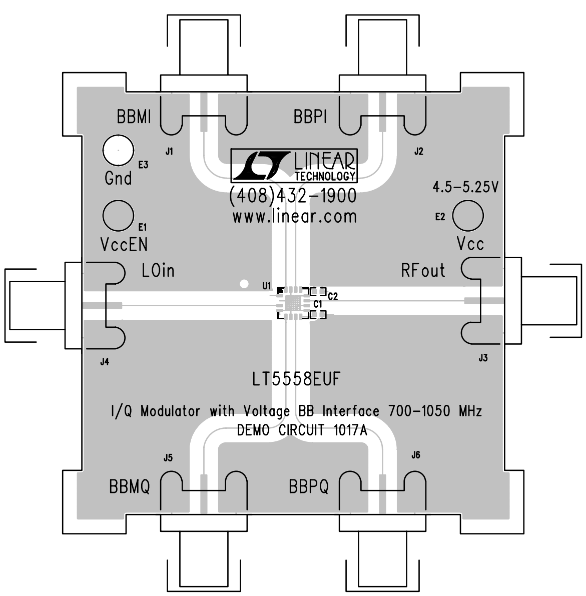


Figure 8. Component Side of Evaluation Board

Application Measurements

The LT5558 is recommended for base-station applications using various modulation formats. Figure 10 shows a typical application.

Figure 11 shows the ACPR performance for CDMA2000 using one and three channel modulation. Figures 12 and 13 illustrate the 1- and 3-channel CDMA2000 measurement. To calculate ACPR, a correction is made for the spectrum analyzer noise floor (Application Note 99).

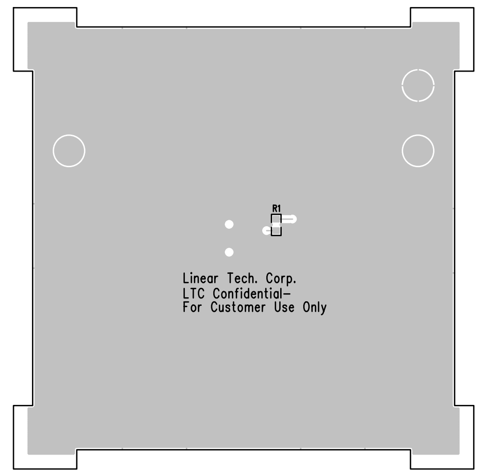


Figure 9. Bottom Side of Evaluation Board

If the output power is high, the ACPR will be limited by the linearity performance of the part. If the output power is low, the ACPR will be limited by the noise performance of the part. In the middle, an optimum ACPR is obtained.

Because of the LT5558's very high dynamic-range, the test equipment can limit the accuracy of the ACPR measurement. Consult Design Note 375 or the factory for advice on ACPR measurement if needed.

The ACPR performance is sensitive to the amplitude mismatch of the BBIP and BBIM (or BBQP and BBQM) inputs. This is because a difference in AC current amplitude will give rise to a difference in amplitude between the even-order harmonic products generated in the internal V-I converter. As a result, they will not cancel out entirely. Therefore, it is important to keep the amplitudes at the BBIP and BBIM (or BBQP and BBQM) inputs as equal as possible.

LO feedthrough and image rejection performance may be improved by means of a calibration procedure. LO feedthrough is minimized by adjusting the differential DC offset at the I and the Q baseband inputs. Image rejection can be improved by adjusting the gain and the phase difference between the I and the Q baseband inputs. The LO feedthrough and Image Rejection can also change as a function of the baseband drive level, as depicted in Figure 14.

APPLICATIONS INFORMATION

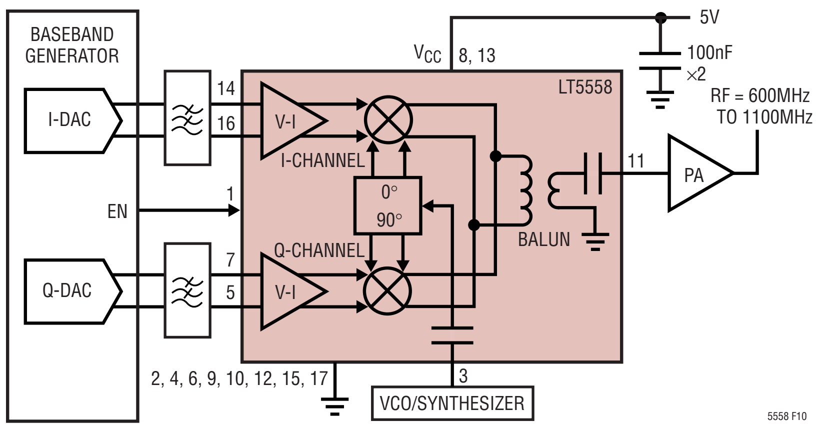


Figure 10. 600MHz to 1.1GHz Direct Conversion Transmitter Application

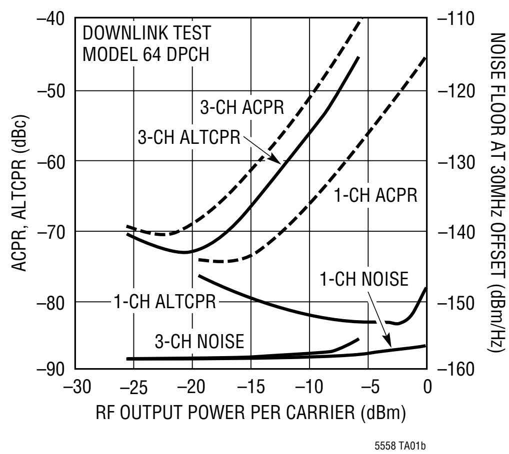


Figure 11. ACPR, ALTCPR and Noise for CDMA2000 Modulation

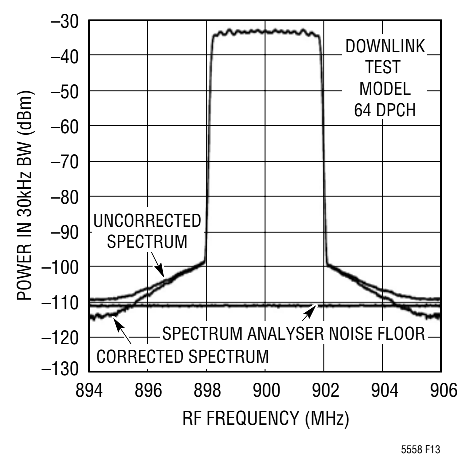


Figure 13. 3-Channel CDMA2000 Spectrum

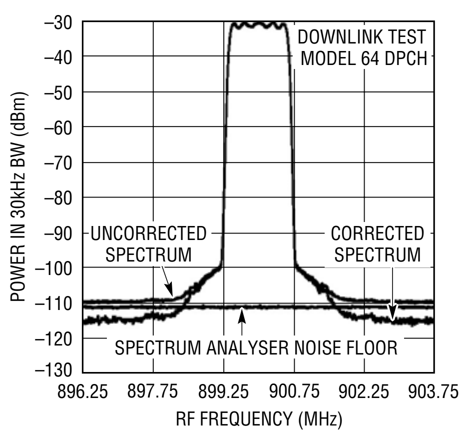


Figure 12. 1-Channel CDMA2000 Spectrum

Example: RFID Application

In Figure 15 the interface between the LTC1565 (U2, U3) and the LT5558 is designed for RFID applications. The LTC1565 is a seventh-order, 650kHz, continuous-time, linear-phase, lowpass filter. The optimum output common-mode level of the LTC1565 is about 2.5V and the optimum input common-mode level of the LT5558 is around 2.1V and is temperature dependent. To adapt the common-mode level of the LTC1565 to the LT5558, a level shift network consisting of R1 to R6 and R11 to R16 is used. The output common-mode level of the LTC1565 can be adjusted by overriding the internally generated voltage on pin 3 of the LTC1565.

APPLICATIONS INFORMATION

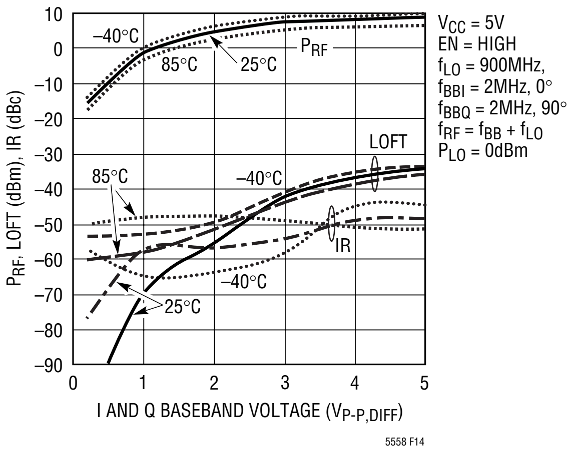


Figure 14. LO Feedthrough and Image Rejection vs Baseband Drive Voltage After Calibration at 25°C

The common-mode voltage on the LT5558 is sampled using resistors R7, R8, R17 and R18 and shifted up to about 2.5V using resistor R9. Op amp U4 compensates for the gain loss in the resistor networks and provides a low-ohmic drive to steer the common-mode input pins of U2 and U3. Resistors R20 and R21 improve op amp U4's stability while driving the large supply decoupling capacitors C3 and C4. This corrected common-mode voltage is applied to the common-mode input pins of U2 and U3 (pins 3). This results in a positive feedback loop for the common mode voltage with a loop gain of about -10dB. This technique ensures that the current compliance on the baseband input pins of the LT5558 is not exceeded under supply voltage or temperature extremes, and internal diode voltage shifts or combinations of these. The core current of the LT5558 is thus maintained at its designed level for optimum performance. The recommended common-mode voltage applied to the inputs of the LTC1565 is about 2V. Resistor tolerances are recommended 1% accuracy or better. The total current consumption is about 160mA and the noise floor at 20MHz offset is –147dBm/Hz with 3.7dBm RF output power. For a $2V_{PP,\ DIFF}$ baseband input swing, the output power at $f_{LO} + f_{BB}$ is 1.6dBm and the third harmonic at $f_{LO} – 3f_{BB}$ is –48.6dBm. For a $2.6V_{PP,\ DIFF}$ input, the output power at $f_{LO} + f_{BB}$ is 3.8dBm and the third harmonic at $f_{LO} – 3f_{BB}$ is –40.5dBm.

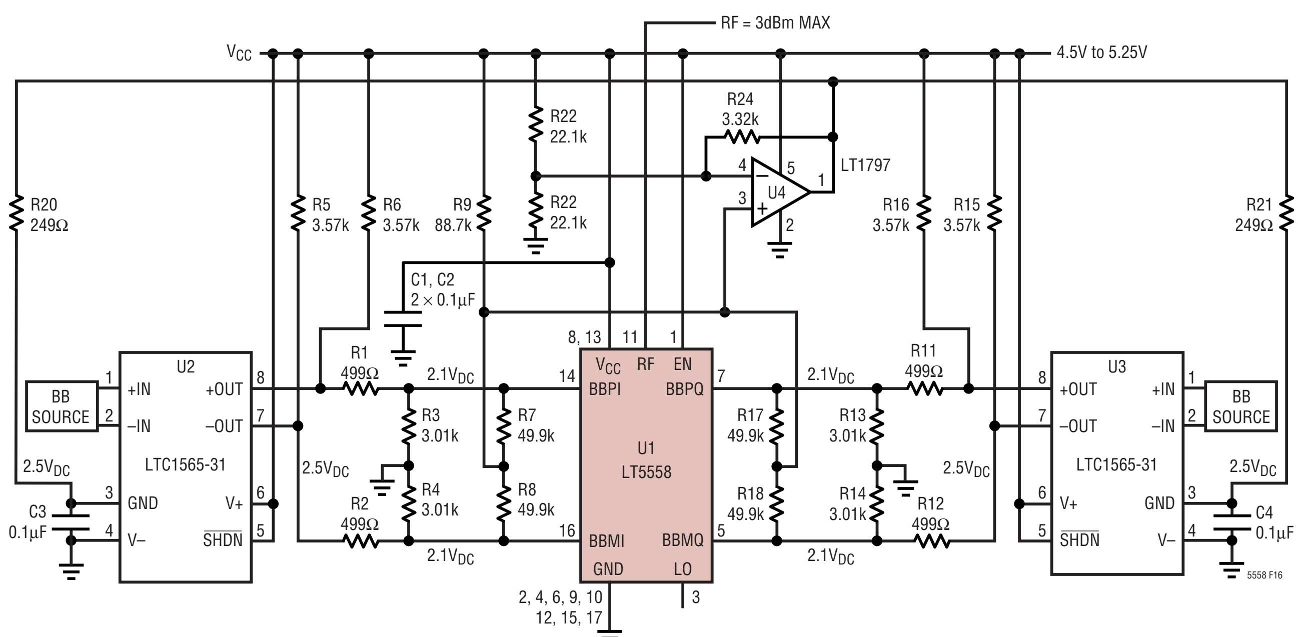
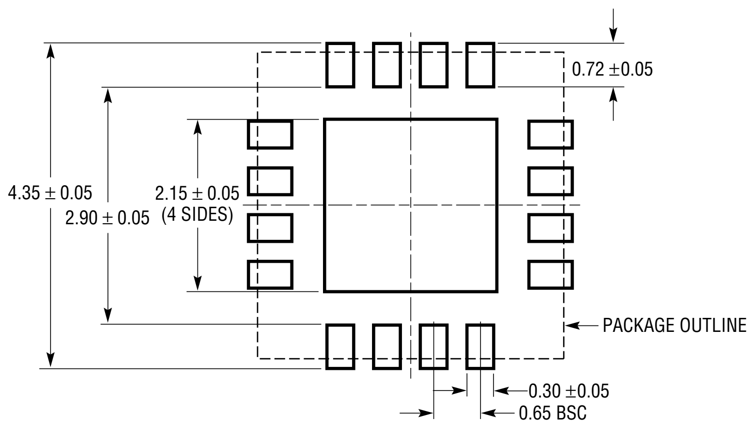


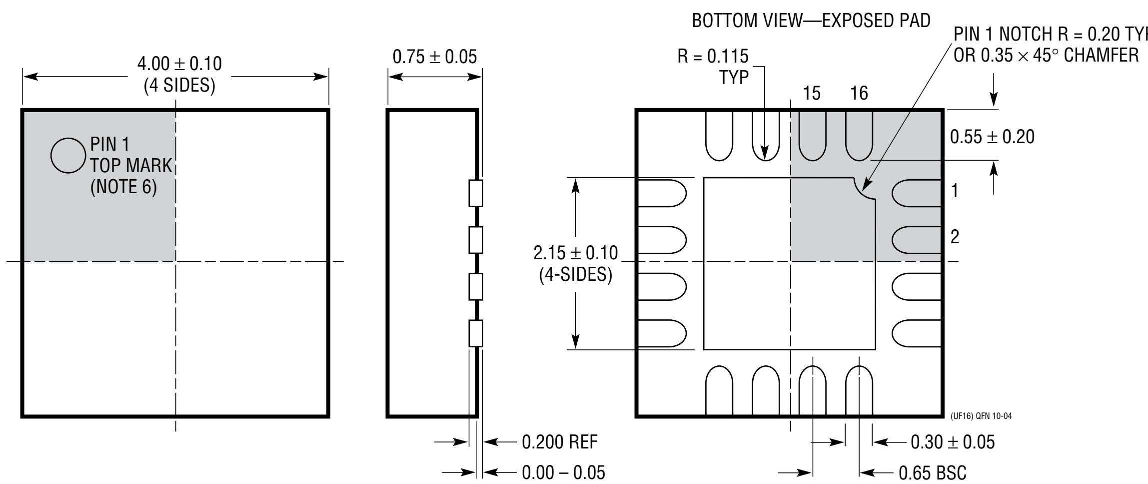
Figure 15. Baseband Interface Schematic of the LTC1565 with the LT5558 for RFID applications.

PACKAGE DESCRIPTION

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5511	High Linearity Upconverting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5512	DC to 3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion, IF Amplifier/ADC Driver with Digitally Controlled Gain	850MHz Bandwidth, 47dBm OIP3 at 100MHz, 10.5dB to 33dB Gain Control Range
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	20dBm IIP3, Integrated LO Quadrature Generator
LT5516	0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator	21.5dBm IIP3, Integrated LO Quadrature Generator
LT5517	40MHz to 900MHz Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5518	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	22.8dBm OIP3 at 2GHz, –158.2dBm/Hz Noise Floor, 50Ω Single-Ended LO and RF Ports, 4-Ch W-CDMA ACPR = –64dBc at 2.14GHz
LT5519	0.7GHz to 1.4GHz High Linearity Upconverting Mixer	17.1dBm IIP3 at 1GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5520	1.3GHz to 2.3GHz High Linearity Upconverting Mixer	15.9dBm IIP3 at 1.9GHz, Integrated RF Output Transformer with 50Ω Matching, Single-Ended LO and RF Ports Operation
LT5521	10MHz to 3700MHz High Linearity Upconverting Mixer	24.2dBm IIP3 at 1.95GHz, NF = 12.5dB, 3.15V to 5.25V Supply, Single-Ended LO Port Operation
LT5522	600MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5524	Low Power, Low Distortion ADC Driver with Digitally Programmable Gain	450MHz Bandwidth, 40dBm OIP3, 4.5dB to 27dB Gain Control
LT5526	High Linearity, Low Power Downconverting Mixer	3V to 5.3V Supply, 16.5dBm IIP3, 100kHz to 2GHz RF, NF = 11dB, I_{CC} = 28mA, –65dBm LO-RF Leakage
LT5527	400MHz to 3.7GHz High Signal Level Downconverting Mixer	IIP3 = 23.5dBm and NF = 12.5dB at 1900MHz, 4.5V to 5.25V Supply, I_{CC} = 78mA
LT5528	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	21.8dBm OIP3 at 2GHz, –159.3dBm/Hz Noise Floor, 50Ω, 0.5V_{DC} Baseband Interface, 4-Ch W-CDMA ACPR = –66dBc at 2.14GHz
LT5568	700MHz to 1050MHz High Linearity Direct Quadrature Modulator	22.9dBm OIP3 at 850MHz, –160.3dBm/Hz Noise Floor, 50Ω, 0.5V_{DC} Baseband Interface, 3-Ch CDMA2000 ACPR = –71.4dBc at 850MHz
LT5572	1.5GHz to 2.5GHz High Linearity Direct Quadrature Modulator	21.6dBm OIP3 at 2GHz, –158.6dBm/Hz Noise Floor, High-Ohmic 0.5V_{DC} Baseband Interface, 4-Ch W-CDMA ACPR = –67.7dBc at 2.14GHz
RF Power Detectors		
LT5504	800MHz to 2.7GHz RF Measuring Receiver	80dB Dynamic Range, Temperature Compensated, 2.7V to 5.25V Supply
LTC®5505	RF Power Detectors with >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5507	100kHz to 1000MHz RF Power Detector	100kHz to 1GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5508	300MHz to 7GHz RF Power Detector	44dB Dynamic Range, Temperature Compensated, SC70 Package
LTC5509	300MHz to 3GHz RF Power Detector	36dB Dynamic Range, Low Power Consumption, SC70 Package
LTC5530	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Gain
LTC5531	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Shutdown, Adjustable Offset
LTC5532	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset
LT5534	50MHz to 3GHz Log RF Power Detector with 60dB Dynamic Range	±1dB Output Variation over Temperature, 38ns Response Time
LTC5536	Precision 600MHz to 7GHz RF Detector with Fast Comparater	25ns Response Time, Comparator Reference Input, Latch Enable Input, –26dBm to +12dBm Input Range
LT5537	Wide Dynamic Range Log RF/IF Detector	Low Frequency to 800MHz, 83dB Dynamic Range, 2.7V to 5.25V Supply
High Speed ADCs		
LTC2220-1	12-Bit, 185Msps ADC	Single 3.3V Supply, 910mW Consumption, 67.5dB SNR, 80dB SFDR, 775MHz Full Power BW
LTC2249	14-Bit, 80Msps ADC	Single 3V Supply, 222mW Consumption, 73dB SNR, 90dB SFDR
LTC2255	14-Bit, 125Msps ADC	Single 3V Supply, 395mW Consumption, 72.4dB SNR, 88dB SFDR, 640MHz Full Power BW

5558fa

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